setting $s = 0$;

if $((N_t \geq N_{sys}) \& (flag = 1))$ then setting $s = 1$;

setting $r = r + 1$; and

if $n > r_N$, resetting n to 1 and repeating step b).

7. The method of claim 1, further comprising the step of bit priority mapping of systematic bits to position of higher reliability in a modulation constellation.

8. The method of claim 7, wherein the mapping step includes providing an interleaver of size $N_{row} \times N_{col}$, where $N_{row}=log_2(M)$ and $N_{col}=N_{trans}/N_{row}$, where M is the modulation size and N_{trans} is the number of coded and rate-matched bits to be transmitted and the upper rows of the array have a higher priority than the lower rows of the array, and wherein data is read into the interleaver, filling the interleaver with all the systematic bits first, followed by the parity bits, and reading data out of the interleaver column by column.

9. The method of claim 8, wherein the interleaver is of size 16x30, and wherein the mapping step includes performing inter-column permutation using the following permutation pattern {0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17}.

10. The method of claim 1, further comprising the step of transmitting a set of parameters governing a selected incremental redundancy version sequence operable in the puncturing steps, the transmitting step including one of the group consisting of: explicitly specifying the redundancy version parameters and transmitting these parameters using a control channel, and initially transmitting a table of redundancy version parameters and then selecting a table entry as a means of identifying the redundancy version parameters.

if $(N_t \geq \frac{1}{BR} \times N_{sys})$ then setting $flag = 1$ and $(N_t = N_t - \frac{1}{BR} \times N_{sys})$ where N_{sys} is the number of systematic bits generated by the turbo encoder;

setting $s = 0$;

if $((N_t \geq N_{sys}) \,\&\, (flag = 1))$ then setting $s = 1$;

setting $r = r + 1$; and

if $n > r_N$, resetting n to 1 and repeating step b).

15. The method of claim 11, further comprising the step of bit priority mapping of systematic bits to position of higher reliability in a modulation constellation, wherein the mapping step includes providing an interleaver of size $N_{row} \times N_{col}$, where $N_{row}=log_2(M)$ and $N_{col}=N_{trans}/N_{row}$, where M is the modulation size and N_{trans} is the number of coded and rate-matched bits to be transmitted and the upper rows of the array have a higher priority than the lower rows of the array, and wherein data is read into the interleaver, filling the interleaver with all the systematic bits first, followed by the parity bits, and reading data out of the interleaver column by column.

16. The method of claim 15, wherein the interleaver is of size 16x30, and wherein the mapping step includes performing inter-column permutation using the following permutation pattern {0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17}.

22. The coder of claim 17, further comprising:

a bit priority mapper coupled to the rate matching block, the bit priority mapper operable to map systematic bits to positions of higher reliability in a modulation constellation;

a symbol interleaver coupled to the bit priority mapper, the interleaver operable to load the systematic symbols and parity symbols into an array in a row-wise manner.

23. The coder of claim 22, wherein interleaver provides an array of size $N_{row} \times N_{col}$, where $N_{row}=log_2(M)$ and $N_{col}=N_{trans}/N_{row}$, where M is the modulation size and N_{trans} is the number of coded and rate-matched bits to be transmitted, and the upper rows of the array have a higher priority than the lower rows of the array, and wherein the bit priority mapper provides data into the interleaver, filling the interleaver with all the systematic bits first, followed by the parity bits, and wherein the interleaver outputs data column by column.

24. The coder of claim 23, wherein the interleaver is of size 16x30, and wherein the bit mapper performs inter-column permutation using the following permutation pattern {0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17}.